In the Drawings

The attached replacement and annotated sheet(s) of drawings include changes to FIGS. 3A – 3D, which have been amended to provide the legend "PRIOR ART."

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS

The Office Action mailed December 16, 2004 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Drawings

The drawing figures have been corrected in accordance with the Examiner's suggestions. Specifically, the legend "PRIOR ART" has been added to FIGS. 3A – 3D. No new matter has been introduced. Approval of the corrections is respectfully requested.

Election Requirement

Applicants affirm the election, without traverse, to prosecute the invention of Group I, Claims 1 – 17 and 27 - 51. Applicants reserve the right to pursue the patentability of the subject matter of the non-elected claims.

Canceled Claims

Claims 33, 34, 45 and 46 have been canceled without prejudice or disclaimer of the subject matter contained therein.

Objection to the Specification

The specification was objected to because of its alleged failure to support some of the subject matter of Claims 33 and 45. Claims 33 and 45 have been canceled. The subject matter of Claim 33 has been incorporated into Claims 35 – 36, which have been re-written in independent form; the subject matter of Claim 45 has been incorporated into Claims 47 – 48, which have been re-written in independent form. Support for the subject matter of Claims 35 – 36 and 47 – 48 can be found for example in paragraphs [0008] and [0011], wherein it is stated that the circuit characteristics that can be matched are "signal delay, clock timing, frequency response, gain, offset, and/or transfer function." FIG. 13 and the corresponding discussion in paragraphs [0034] – [0036] relate to adjustment of gain mismatching. Paragraph [0037] relates to the matching of the circuit characteristic of signal pathways. Paragraph [0038] relates to the matching of the circuit characteristic of input offset, and so forth.

Rejection(s) Under 35 U.S.C. § 112, Second Paragraph

Claims 12 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claim 12 has been amended to clarify that first and second transistors are intended and to provide antecedent basis for same.

Rejection(s) Under 35 U.S.C. § 103

Claims 1 – 17 and 25 – 51 were rejected under 35 U.S.C. § 103(a) as unpatentable over allegedly admitted prior art (AAPA) in view of Kliza et al. (U.S. pat. no. 5,852,640).

Claims 1, 4, 8, 10, 12, 16, 27, 30 and 32 have been amended to recite a mechanism by which delay is effected using charge storage in a floating gate of a transistor. For example, Claim 1 was amended to recite a time-interleaved system operable to distribute a signal into a first processing pathway and, following a predetermined amount of time, into a second processing pathway,

> wherein the predetermined amount of time depends on an amount of electrical charge stored on the floating gate of [an] at least one floating-gate field effect transistor, said amount of electrical charge adjusting a slew rate of an output of the delay structure to thereby controllably influence a triggering time of a circuit associated with at least one of the first and second processing pathways.

This mechanism is neither disclosed nor suggested in AAPA and Kliza et al., considered singularly or in combination. Kliza et al. is directed to a system for compensating for propagation time differences in signal pathways, so that clock signals traveling along these pathways reach intended subsystems in precisely timed intervals. Compensation is accomplished using adjustable delay elements AD. In the paragraph bridging columns 15 and 16 referenced in the Office Action, Kliza et al. states that rather than undergo a learning process to establish the values of the delay elements AD each time the system is powered up, these values can be stored in a non-volatile memory preferably in the form of an EEPROM or a flash memory. The storage

mechanism, according Kliza et al., is "the memory's floating gate [used] as a continuous charge storage device."

Applicants respectfully maintain that Kliza et al.'s use of an EEPROM's or flash memory's floating gate as a storage mechanism is consistent with conventional uses of such storage devices, and is distinct from the claimed mechanism. Specifically, there is no discussion in Kliza et al. of using stored charge on a floating gate to adjust a slew rate of an output of a delay structure to thereby controllably influence a triggering time of a circuit. Kliza et al. fails to mention slew rate, but instead delays the time it takes a clock signal to reach a target subsystem. Therefore, even if Kliza et al. were properly combinable with APA, the result would be a different mechanism than that claimed. For this reason at least, the obviousness rejection of Claims 1, 4, 8, 10, 12, 16, 27, 30 and 32, and the claims dependent therefrom, is improper and should be withdrawn.[1]

Claims 35 and 36 have been amended to include the limitations of base Claim 33. Claims 47 and 48 have been amended to include the limitations of base Claim 45. Claim 35 and

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[1] According to the Manual of Patent Examining Procedure (M.P.E.P.),

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must

47 relate to matching relative gains of circuit elements in first and second circuit pathways. Claim 36 and 48 relate to matching frequency response, offset or transfer functions of first and second circuit pathways. With respect to Claims 35, 36, 47 and 48, the Office Action contends that "since the claimed structure is met by the reference, inherently, the result functions of these claims will also be met." Applicants respectfully disagree. Simply because a structure that is similar to the prior art is claimed does not imply that all the claimed limitations are disclosed in the prior art. There are numerous instances of devices that use similar structures but that perform very different functions. A field effect transistor can be biased in many different ways and used in many different contexts, for example, to achieve very different functions, from memory devices to amplifiers, switches, and so forth, and one use does not necessarily suggest or anticipate another. In the instant case, the recited functions of matching relative gains (Claims 35 and 47) and matching frequency response, offset or transfer functions (Claims 36 and 48) are neither disclosed nor suggested by Kliza et al., even though Kliza et al. discloses the use of an EEPROM and flash memory, which are conventional devices utilizing floating gate devices. It is respectfully urged therefore that the obviousness rejection of these 35, 36, 47 and 47, and the claims dependent therefrom, is improper and its withdrawal is respectfully requested.

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both be found in the prior art, not in the applicant's disclosure. M.P.E.P. § 2143.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fee, including those necessary to obtain extensions of time to render timely the filing of the instant Reply, or credit any overpayment not otherwise paid or credited, to our deposit account No. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.

Dated: 3/16/05

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ANNOTATED SHEET

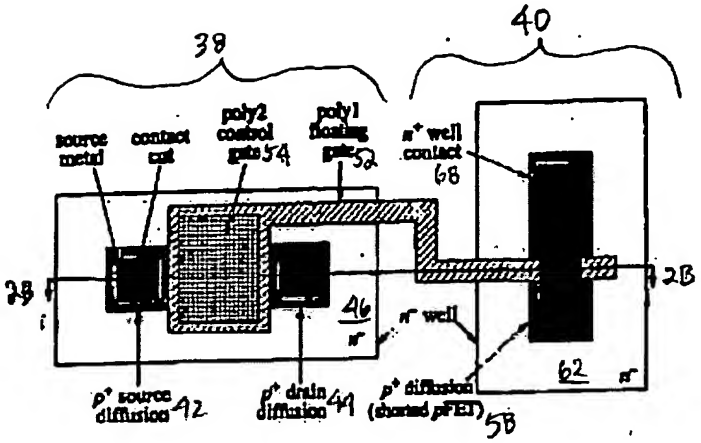

FIG. 3A
(PRIOR ART)

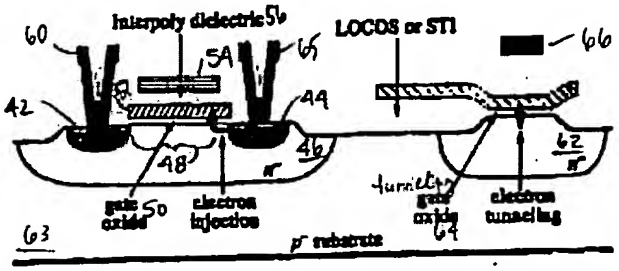

FIG. 3B
(PRIOR ART)

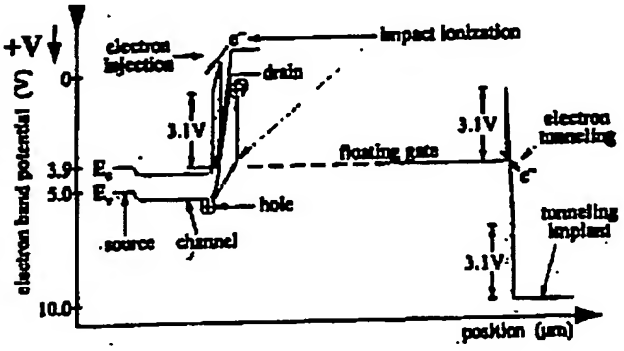

FIG. 3C
(PRIOR ART)

ANNOTATED SHEET

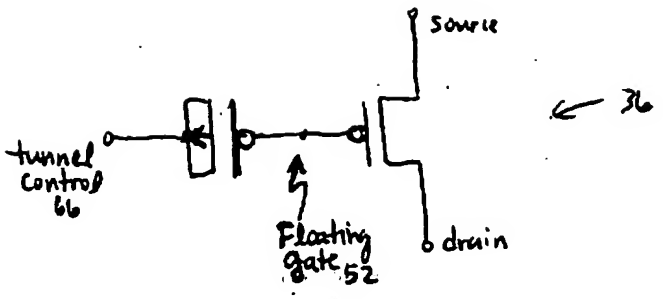

FIG. 3D
(PRIOR ART)